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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/002,085	11/01/2001	William John Goetzinger	ROC920010202US1	2023

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EXAMINER	
AHMED, SALMAN	
ART UNIT	**PAPER NUMBER**
2616	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/19/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/002,085	GOETZINGER ET AL.	
	Examiner	Art Unit	
	Salman Ahmed	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12/26/2006 (RCE)*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *5-7, 9-12, 17-19, 22 and 25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *5-7,9-12,17-19,22 and 25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11/1/2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claims 5-7, 9-12, 17-19, 22 and 25 are pending.

Claims 5-7, 9-12, 17-19, 22 and 25 are rejected.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 5-7, 9-12, 17-19 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 5, the limitation "determining if an empty indicator of a scheduling queue is set to empty" and limitation "searching the scheduling queue if the empty indicator indicates that a flow is associated with the scheduling queue" fails to particularly point out and distinctly claim the subject matter which applicant regards as the invention, because, it is not clear the relationship between determining if an empty indicator being empty, and empty indicator indicating that a flow is associated with the scheduling queue. Does, empty indicator means queue is empty or does it mean queue has no flow in it. As such it is confusing as to the functionality of the empty indicator.

Claims 19 and 22 have similar problem. The limitation determining if and empty indicator of a scheduling queue is set to empty and limitation searching the scheduling queue if the empty indicator indicates that a flow is associated with the scheduling queue fails to particularly point out and distinctly claim the subject matter

which applicant regards as the invention, because, it is not clear the relationship between determining if an empty indicator being empty, and empty indicator indicating that a flow is associated with the scheduling queue. Does, empty indicator means queue is empty or does it mean queue has no flow in it. As such it is confusing as to the functionality of the empty indicator.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Meier et al. (U.S. 6,481,251), hereinafter referred in view of Yoneda (US PAT PUB 2002/0024830)

In regards to claim 5, Meier teaches a method of dequeuing a flow (to be hit by the load) from a scheduling queue (store queue) the method comprising: searching the scheduling queue if empty indicator indicates that a flow is associated with the scheduling queue; determining if the scheduling queue is empty based on the search; (column 14, lines 60-67 and column 15, lines 7-10, Meier teaches store queue control circuit 74 generates a mask using the load's store queue number and the head store queue number (step 120). The mask includes a bit for each store queue entry. The bit is set if the store queue entry is eligible to be hit by the load (i.e. the entry is between the head entry indicated by the head store queue number and the entry indicated by the load's store queue number), and is clear if the store queue entry in not eligible to be hit by the load. In other words, store queue control circuit 74 determines if there is still a hit signal asserted after masking via step 122. If so, data is forward to D-cache 44 from the hit entry (step 126)).

Meier does not explicitly teach the queue having empty indicator and setting the empty indicator to empty if the search determines that the scheduling queue is empty and further detaching the flow associated with the scheduling queue found when the scheduling queue is searched.

Yoneda, in the same field of endeavor teaches (page 2 section 0023) the erasure of data means that, for example, one bit in the word memory is allocated as a bit (empty

bit) that is used to determine the existence of data, and the bit is overwritten so as to be converted from logic representing a data-existence to logic representing a data-nonexistence. In addition, each of the word memories may have an empty flag as a flipflop that indicates whether valid data is stored or not in the word memory, and data can be erased by overwriting the flag). Yoneda further teaches (page 3 section 0045) alternatively, the data may be erased in the following method. An empty flag is provided as a flipflop in each of the word memories. The flipflop indicates whether valid data is stored in the word memory. The data is erased by overwriting the flag.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Meier's teaching by incorporating the steps the empty indicator being in the queue and setting the empty indicator to empty if the search determines that the scheduling queue is empty and further detaching the flow associated with the scheduling queue found when the scheduling queue is searched as suggested by Yoneda. The motivation is that such method will enable to a process not waste processing time by going through memories that do not contain data; thus making the system efficient.

6. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Meier and Yoneda as applied to claims 5, further in view of Applicant's admitted prior art.

Regarding claim 6, Meier and Yoneda teach empty indicator associated with scheduling queue for scheduling purpose as described in the rejections of claim 5 above.

Meier and Yoneda do not explicitly teach, selecting the scheduling queue from among a plurality of scheduling queues in a round robin process.

Applicant's admitted prior art teaches (page 8 lines 1-2) selecting the scheduling queue from among a plurality of scheduling queues in a round robin process

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify Meier and Yoneda's method by incorporating the steps of searching the scheduling queue in a round robin as suggested by Applicant's admitted prior art. The motivation is that Round-Robin process lets all queues get fair scheduling and helps efficient transmission of data.

7. Claims 7, 9, 11, 12, 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Meier and Yoneda as applied to claim 5 above, further in view of Naven et al. (U.S. 6,810,043), hereinafter referred to as Naven.

Regarding claim 7, Meier and Yoneda teach teach empty indicator associated with scheduling queue for scheduling purpose as described in the rejections of claim 5 above.

Meier and Yoneda do not explicitly teach searching step includes a plurality of sub-queues includes in the scheduling queue, the sub-queues having mutually different respective ranges and resolutions.

Naven in the same field of endeavor teaches that the master calendar (scheduling queue) and slave calendar (sub-queues) are plurality of storage locations corresponding respectively to a succession of time slots (column 4 lines 44-45). It can

also be seen from figure 2 that the slave calendar and master calendar have a different number of time slots.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify Meier and Yoneda's method by incorporating the method of having different ranges and resolutions for sub-queues as taught by Naven. A motivation for doing so would be the master calendar and slave calendar have the different range and resolution of slots (the scheduling queue has different number of slots that is different than a number slots of the sub-queue, 7 and 2 of figure 2). This would make the system hierarchal and would help implement efficient network management.

Regarding claim 9, Meier and Yoneda do not explicitly teach attaching a flow to the scheduling queue; and placing the empty indicator associated with the scheduling queue in a condition to indicate that the scheduling queue is not empty.

Naven in the same field of endeavor teaches "attaching a flow to the scheduling queue" Naven teaches each storage location 2 is capable of storing one or more entries, each such entry denoting that a specified virtual channel is to be serviced by the traffic manager in the time slot which the storage location corresponds as stated in column 1, lines 58-61. "Placing an empty indicator associated with the scheduling queue in a condition to indicate that the scheduling queue is not empty." Naven discloses the master snoop memory 20 is N bits wide such that each N-bit word 22 corresponds individually to one of the storage locations 2 of the group. In this case,

when a bit in the word 22 is set to 1, this denotes that the corresponding storage location 2 has at least one VC entered therein.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify Meier and Yoneda's method by incorporating the steps of attaching a flow to the scheduling queue; and placing the empty indicator associated with the scheduling queue in a condition to indicate that the scheduling queue is not empty as suggested by Naven. The motivation is that such method will enable to a process not waste processing time by going through memories that do not contain useable data; thus making the system efficient.

In regards to claims 11, Meier teaches the placing step includes setting a bit in a register (column 14 lines 1-6, Finally, if the empty indication in the empty register indicates that the store queue is empty, the empty indication is set to indicate not empty (step 90). For example, the empty indication may be a bit indicating empty when set and indicating not empty when clear).

In regards to claims 12, Meier teaches the placing step includes resetting a bit in a register (column 14 lines 1-6, Finally, if the empty indication in the empty register indicates that the store queue is empty, the empty indication is set to indicate not empty (step 90). For example, the empty indication may be a bit indicating empty when set and indicating not empty when clear).

In regards to claim 17, Meier and Yoneda do not explicitly teach detaching step is performed, a further search of the scheduling queue is performed to determine whether

any flows are enqueued in the scheduling queue other than the flow detached in the detaching step.

Naven in the same field of endeavor discloses if the detaching step is performed, a further search of the scheduling queue is performed to determine whether any flows are en-queued in the scheduling queue other than the flow detached in the detaching step' (Column 8, lines 24-28, when a bit in the word 22 is set to 1 this denotes that the corresponding storage location 2 has at least one VC entered therein. If the bit is 0, on the other hand, this denotes that the corresponding storage location 2 is "empty" i.e. does not contain a valid entry).

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify Meier and Yoneda's method by incorporating the method of doing further search and setting an indicator as taught by Naven. The motivation is that such additional search will help prevent race condition, i.e. during first search if the state of the queue changes, it will be detected; thus making the system more robust and less error prone.

In regards to claims 18, Meier and Yoneda do not explicitly teach empty indicator is placed in a condition to indicate that the scheduling queue is empty if the further search of the scheduling queue determines that there are no flows in the scheduling queue other than the flow detached in the detaching step.

Naven in the same field of endeavor discloses "the empty indicator is placed in a condition to indicate that the scheduling queue is empty if the further search of the scheduling queue determines that there are no flows in the scheduling queue other than

the flow detached in the detaching step (column 8, lines 26-28, if the bit is 0, on the other hand, this denotes that the corresponding storage location 2 is "empty", i.e. does not contain a valid entry).

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify Meier and Yoneda's method by incorporating the method of doing further search and setting an indicator as taught by Naven. The motivation is that such additional search will help prevent race condition, i.e. during first search if the state of the queue changes, it will be detected; thus making the system more robust and less error prone.

8. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Meier, Yoneda and Naven as applied to claim 9, further in view of Applicant's admitted prior art.

Regarding claim 10, Meier, Yoneda and Naven teach empty indicator associated with scheduling queue for scheduling purpose as described in the rejections of claim 9 above.

Meier, Yoneda and Naven do not explicitly teach the attaching step includes assigning the flow to a slot in the scheduling queue according to the formula CP + ([WF x FS)/SF), where: CP is a pointer that indicates a current position in the scheduling queue; WF is a weighting factor associated with the flow; FS is a size of a data frame associated with the flow; and SF is a scaling factor.

Applicant's admitted prior art teaches assigning the flow to a slot in the scheduling queue according to the formula CP + ([WF x FS)/SF), where: CP is a pointer that indicates a current position in the scheduling queue; WF is a weighting factor associated with the flow; FS is a size of a data frame associated with the flow; and SF is a scaling factor.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify Meier, Yoneda and Naven's method by incorporating the steps of assigning the flow to a slot in the scheduling queue according to the formula CP + ([WF x FS)/SF), where: CP is a pointer that indicates a current position in the scheduling queue; WF is a weighting factor associated with the flow; FS is a size of a data frame associated with the flow; and SF is a scaling factor as suggested by Applicant's admitted prior art. The motivation is that (as suggested by the Applicant's admitted prior art, page 7 first paragraph) with this known weighted fair queuing technique, the weighting factors assigned to the various flows in accordance with the QoS assigned to each flow govern how close to the current pointer of the queue each flow is enqueued. In addition, flows which exhibit larger frame sizes are enqueued farther from the current pointer of the queue, to prevent such flows from appropriating an undue proportion of the available bandwidth of the queue.

1. Claims 19 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicants admitted prior art in view of Yoneda and Meier.

Regarding claim 19 "network processor, comprising:" Applicant's

admitted Prior Art Figure 1 teaches network processor (28,30) "one or more scheduling queues, each adapted to define a respective sequence in which flows are to be serviced". Admitted Prior Art Figure 2 teaches scheduler queue and sequence of data flow 42.

In regards to claim 22, Applicant's admitted prior art further teaches a computer program, the computer program product comprising: a medium readable by a computer, the computer readable medium having computer program code (Figure 1, page 2 paragraph 4 to end of page 3).

In regards to claims 19 and 22, Applicant's Admitted Prior Art fails to explicitly teach one or more empty indicators, each empty indicator being associated with a respective scheduling queue to indicate whether the respective scheduling queue is empty.

Yoneda, in the same field of endeavor teaches (page 2 section 0023) the erasure of data means that, for example, one bit in the word memory is allocated as a bit (empty bit) that is used to determine the existence of data, and the bit is overwritten so as to be converted from logic representing a data-existence to logic representing a data-nonexistence. In addition, each of the word memories may have an empty flag as a flipflop that indicates whether valid data is stored or not in the word memory, and data can be erased by overwriting the flag). Yoneda further teaches (page 3 section 0045) alternatively, the data may be erased in the following method. An empty flag is provided as a flipflop in each of the word memories. The flipflop indicates whether valid data is stored in the word memory. The data is erased by overwriting the flag.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Applicant's Admitted prior art teaching by incorporating the steps one or more empty indicators, each empty indicator being associated with a respective scheduling queue to indicate whether the respective scheduling queue is empty as suggested by Yoneda. The motivation is that such method will enable to a process not waste processing time by going through memories that do not contain data; thus making the system efficient.

Applicant's admitted prior art and Yoneda do not explicitly teach determining if an empty indicator is set to empty; search the scheduling queue if the empty indicator indicates that a flow is associated with the scheduling queue; determine if the scheduling queue is empty based on the search; set the empty indicator to empty if the search determines that the scheduling queue is empty; and detach the flow associated with the scheduling queue wherein the flow is found when the scheduling queue is searched.

Meier in the same field of endeavor teaches (column 14, lines 60-67 and column 15, lines 7-10) store queue control circuit 74 generates a mask using the load's store queue number and the head store queue number (step 120). The mask includes a bit for each store queue entry. The bit is set if the store queue entry is eligible to be hit by the load (i.e. the entry is between the head entry indicated by the head store queue number and the entry indicated by the load's store queue number), and is clear if the store queue entry in not eligible to be hit by the load. In other words, store queue control

circuit 74 determines if there is still a hit signal asserted after masking via step 122. If so, data is forward to D-cache 44 from the hit entry (step 126)).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Applicant's Admitted prior art and Yoneda's teaching by incorporating the steps determining if an empty indicator is set to empty; search the scheduling queue if the empty indicator indicates that a flow is associated with the scheduling queue; determine if the scheduling queue is empty based on the search; set the empty indicator to empty if the search determines that the scheduling queue is empty; and detach the flow associated with the scheduling queue wherein the flow is found when the scheduling queue is searched as suggested by Meier. The motivation is that such method will enable to a process not waste processing time by going through memories that do not contain data; thus making the system efficient.

2. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicants admitted prior art in view of Yoneda.

Applicant's admitted prior art teaches a method of enqueuing a flow to a scheduling queue, comprising: attaching a flow to the scheduling queue; and wherein the attaching step includes assigning the flow to a slot in the scheduling queue according to the formula CP + ((WF x FS)/SF), where: CP is a pointer that indicates a current position in the scheduling queue; WF is a weighting factor associated with the flow; FS is a size of a data frame associated with the flow; and SF is a scaling factor (page 7 first paragraph).

Applicant's admitted prior art does not explicitly teach placing an empty indicator of a plurality of empty indicators associated with the queue in a condition to indicate that the queue is not empty.

Yoneda, in the same field of endeavor teaches (page 2 section 0023) the erasure of data means that, for example, one bit in the word memory is allocated as a bit (empty bit) that is used to determine the existence of data, and the bit is overwritten so as to be converted from logic representing a data-existence to logic representing a data-nonexistence. In addition, each of the word memories may have an empty flag as a flipflop that indicates whether valid data is stored or not in the word memory, and data can be erased by overwriting the flag). Yoneda further teaches (page 3 section 0045) alternatively, the data may be erased in the following method. An empty flag is provided as a flipflop in each of the word memories. The flipflop indicates whether valid data is stored in the word memory. The data is erased by overwriting the flag.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Applicant's admitted prior art teaching by incorporating the steps of placing an empty indicator of a plurality of empty indicators associated with the queue in a condition to indicate that the queue is not empty as suggested by Yoneda. The motivation is that such method will enable to a process not waste processing time by going through memories that do not contain data; thus making the system efficient.

Response to Arguments

3. Applicant's arguments related to RCE, see pages 8-13 of the Remarks section, filed 12/26/2006, with respect to the rejections of the claims have been fully considered. Examiner respectfully points out that the Applicant meant to disclose claims 5, 19, 22 and 25 being the only independent claims pending (page 8 first paragraph). Examiners amendments necessitated a new ground of rejections presented in this office action. As such any response to arguments are moot.

Allowable subject matter:

Upon further review of the application and in view of updated search the allowability of claim 10 (now incorporated in claim 25) has been withdrawn.

USC 103 (a) Rejection:

Applicant has amended claims 5, 19 and 22 and added claim 25. The amendments to claims 5, 19 and 22 have changed the scope of the claims. As such a new ground of rejections are presented in this office action. So any response to arguments to claims 5-7, 9-12, 17-19, 22 and 25 are moot.

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Salman Ahmed whose telephone number is (571)272-8307. The examiner can normally be reached on 8:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hassan Kizou can be reached on (571) 272-3088. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Art Unit 2616

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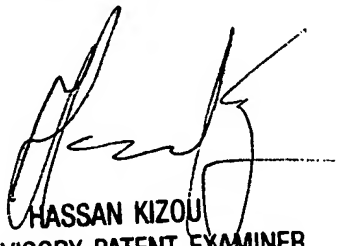
1/24/2007



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